

Remarks:

Reconsideration of the application is requested.

Claims 1-7 remain in the application. Claims 1, 3, and 5 have been amended. A marked-up version of the claims is attached hereto on separate pages.

In item 1 on page 2 under "Drawings" of the above-identified Office Action, the Examiner has objected to the drawings as not complying with PTO 948. Although a copy of PTO 948 was not enclosed with the Office Action, applicants respectfully point out that formal drawings were submitted on March 12, 2002 to the PTO Official Draftsman, a copy of which is enclosed herewith for the Examiner's convenience. Therefore, since the drawings are believed to comply with the PTO requirements, the Examiner is requested to withdraw his objection.

In item 3 on page 2 of the above-identified Office Action, claims 1, 3, and 4-7 have been rejected as being anticipated by Sugino et al. (U.S. Patent Application Pub. No. 2002/0055238) under 35 U.S.C. § 102(e).

The rejection has been noted and claims 1, 3, and 5 have been amended in an effort to even more clearly define the invention of the instant application. In claim 1 the language has been

clarified to recite that all the trenches are filled with the protective material at the same time the protective layer is applied to the bottom surface of the wafer. Support for this change is found in the original disclosure on page 8, lines 3-6 of the instant specification. In claim 3 the language has been clarified to recite that all the trenches are filled at the same time the wafer is mounted on the mounting tape which has the glue layer. Support for this change is found on page 9, lines 14-19 of the instant specification. Claim 5 has been clarified to recite that the protective foil also is in contact with the bottom surface of the wafer. Support for this change is found on page 10, lines 2-10 the instant specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method to apply a protective coating to a bottom surface of a wafer, that includes forming trenches in a top surface of the wafer, applying a protective material on the bottom surface of the wafer, and at the same time filling all of the trenches with the protective material.

The Sugino et al. reference discloses a wafer 1 in which grooves 2 are cut and a surface protective sheet 10 is stuck to cover the surface of the wafer. Sheet 10 has a removable adhesive layer 12 that is curable by energy radiation. The

back of the wafer is ground and divided into individual chips 3. A pressure sensitive adhesive sheet 20 including an energy radiation curable adhesive layer 22 is stuck on the back of the wafer 1 to facilitate maintaining alignment of the chips 3 during a pickup step.

Clearly, Sugino et al. do not show or teach filling the trenches with the protective material as recited in claim 1 or the glue as recited in claim 3 of the instant application.

Sugino et al. disclose in Figs. 4, 5, 6, 8, and 9 and their corresponding description that the tape comprising the adhesive layer is only applied to cover the surface of the wafer. The protective layer does not enter the grooves.

The present invention uses a viscous material, such as glue, that can be hardened, is easily introduced into the sawn trenches, and can be easily cut by a thinner blade than is possible in the prior art. Filling the trenches provides complete protection of all the edges of the individual chips as recited in claims 1 and 3. This complete protection, as claimed, cannot be obtained by simply covering the grooves as shown in Sugino et al.

Independent claim 5 is directed to an alternate embodiment of the present invention in which a protective foil is mounted on

a mounting tape in direct contact with the bottom surface of the wafer. This limitation is neither shown nor taught in Sugino et al.

In item 6 on page 4 of the above-identified Office Action, claim 3 has been rejected as being unpatentable over Sugino et al. (U.S. Patent Application Pub. No. 2002/0055238) under 35 U.S.C. § 103(a). Presumably, the Examiner intended this rejection to apply to claim 2, not claim 3, and inadvertently referred to claim 3. The limitation of "fastening the wafer onto a dicing frame" referred to by the Examiner is recited in claim 2, not in claim 3. Therefore, applicants will direct their remarks and arguments to claim 2.

The Sugino et al. reference is deficient for the reasons discussed above. Further, the Examiner has acknowledged that Sugino et al. do not disclose using a mounting tape to fasten the wafer to a dicing frame, and merely dismisses this claim limitation as "obvious to a person having ordinary skills in the art" without providing any support in the prior art for such an allegation. The Examiner's statement is pure conjecture based on hindsight. Absent a proper prior art teaching this rejection is deemed untenable.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either

show or suggest the features of independent claims 1, 3, and 5. Claims 1, 3, and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 3, or 5.

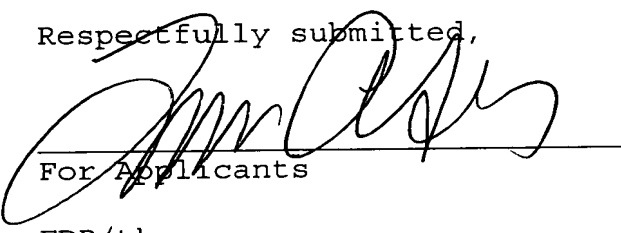
In view of the foregoing, reconsideration and allowance of claims 1-7 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees that might be due with respect to  
Sections 1.16 and 1.17 to the Deposit Account of Lerner and  
Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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Application No. 10/062,942

Version With Markings to Show Changes Made:

Claim 1 (Twice Amended). A method of applying a protective coating to a bottom surface of a wafer, and of protecting bottom edges and corners of chips forming part of the wafer, which comprises the steps of:

forming trenches in a top surface of the wafer;

applying a top side dicing tape to the top surface;

grinding the wafer at a bottom surface opposite the top surface and thereby laying open the trenches;

applying a protective material on the bottom surface and at the same time filling all the trenches to protect the bottom surface and the bottom edges and corners; and

hardening the protective material to form a protection layer.

Claim 3 (Twice Amended). A method of applying a protective coating to a bottom surface of a wafer, and of protecting bottom edges and corners of chips forming part of the wafer, which comprises the steps of:

forming trenches in a top surface of the wafer;

applying a top side dicing tape to the top surface;

grinding the wafer at a bottom surface opposite the top surface and thereby laying open the trenches;

applying a glue layer onto a mounting tape; and

mounting the wafer on the mounting tape and at the same time causing the glue to fill all the trenches to protect the bottom surface and the bottom edges and corners.

Claim 5 (Amended). A method of applying a protective coating to a bottom surface of a wafer, which comprises the following steps:

applying a protective foil onto a mounting tape; and

mounting a bottom surface of the wafer onto the mounting tape with the protective foil facing and in contact with the bottom surface of the wafer to protect the bottom surface thereof.